

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-18 are pending in the present application. Claim 9 is amended and Claims 17 and 18 are added by the present amendment.

In the outstanding Office Action, Claims 9-13 were rejected under 35 U.S.C. § 112, second paragraph, and Claims 1-16 were rejected under 35 U.S.C. § 102(e) as anticipated by Takashima (U.S. Patent No. 6,549,449).

Regarding the rejection of Claims 9-13 under 35 U.S.C. § 112, second paragraph, Claim 9 has been amended to positively recite third and fourth bit lines as shown in Figure 13 and disclosed in the specification at page 18, lines 15-25. Thus, it is respectfully requested this rejection be withdrawn.

Regarding the rejection of Claims 1-16 under 35 U.S.C. § 102(e) as anticipated by Takashima, that rejection is respectfully traversed for the following reasons.

Briefly recapitulating, Claim 1 is directed to a semiconductor integrated circuit that includes, *inter alia*, first and second bit lines, first and second plate lines, a first series connected TC unit type structure having one terminal connected to the first bit line and another terminal connected to the first plate line, a second series connected TC unit type structure connected with one terminal to the second bit line and with another terminal to the second plate line, a plate line potential control circuit, and a bit line potential control circuit. The plate line potential control circuit controls, in a standby state, potentials of the first and second plate lines to have a first potential, and in an active state, the potential of the first plate line to have a second potential and the potential of the second plate line to have a third potential when one of the series connected memory cells included in the first series connected TC unit type structure is selected. The bit line potential control circuit controls a potential of

the second bit line to have the third potential, after charges are transferred from one of the ferroelectric capacitor included in the first series connected TC unit type structure to the first bit line. Independent Claim 14 is similar to Claim 1, except that Claim 14 is a method claim.

Thus, the second bit line is connected to the non-elected second series connected TC unit type structure, the third potential is a potential of the second plate line, and the second plate line is connected to the non-elected second series connected TC unit type structure. Further, after the bit line potential control circuit of the device of Claim 1 transfers charges from the ferroelectric capacitor included in the elected first series connected TC unit type structure, the bit line potential control circuit changes the potential of the second bit line connected to the non-elected second series connected TC unit type structure to the third potential. Thus, the bit line potential control circuit advantageously prevents the destruction of data in the memory cell included in the non-elected second series connected TC unit type structure, as disclosed in the specification at page 12, lines 9-27.

Turning to the applied art, Takashima shows in Figure 17 a first bit line /BL, a second bit line BL, a first plate line /PL, a second plate line PL, a first structure C1, and a second structure (not labeled but below and similar to the first structure C1). However, a bit line potential control circuit, although not identified by the outstanding Office Action with any element of Takashima, can be the circuit receiving the signal HEQL shown in Figure 17. This circuit of Takashima applies a potential V_{aa} to the bit lines BL and /BL, which is at "1" level as shown in Figure 1B.

However, Takashima does not teach or suggest that a potential of the plate lines PL and /PL is V_{aa} . Applicants note that Claim 1 recites that the plate line potential control circuit, in an active state, changes the potential of the second plate line to the third potential and the bit line potential control circuit changes the potential of the second bit line also to the

third potential, thus both the second plate line and the second bit line being at the same third potential, which is different than Takashima.

Therefore, it is respectfully submitted that independent Claims 1 and 14, and each of the claims depending therefrom, patentably distinguish over Takashima.

New Claims 17 and 18 have been added to set forth the invention in a varying scope and Applicants submit the new claims are supported by the originally filed specification. In particular, new Claims 17 and 18 are supported by the specification at page 12, lines 9-27 and depend from independent Claims 1 and 14, which are believed to be allowable as discussed above.

Accordingly, it is respectfully submitted that dependent Claims 17 and 18 are also allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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